UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,040	06/28/2005	Hirokazu Hanaki	SON-2905	1974

23353 7590 08/02/2007

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
08/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/541,040	HANAKI, HIROKAZU	
	Examiner	Art Unit	
	Mark Connolly	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/10/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 have been presented for examination.

2. The objection to the specification and the rejections under 112, first paragraph have been maintained and rebuttal arguments have been included herein.

3. Applicant's arguments with respect to claims 1-9 under 102 and 103 have been considered but are moot in view of the new ground(s) of rejection.

Specification

4. The disclosure is objected to because of the following informalities:

In particular, the DISCLOSURE OF THE INVENTION recites having a *random* gap between clock pulses when a bus busy signal does not indicate a bus busy state. The size of this gap is defined by a count value stored in setting register 21, which is set in advance according to an interrupt factor. Because the gap size is defined, it is not *random*.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1 and 4-6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In particular, the claims recite having a *random* gap between clock pulses when a bus busy signal does not indicate a bus busy state. The size of this gap is defined by a count value

stored in setting register 21, which is set in advance according to an interrupt factor. For examination purposes, because the gap size is defined, it is not interpreted as being *random.*

Claim Objections

7. Claims 2 and 7 are objected to and should be clarified as follows:

For examination purposes, claim 2 has been interpreted as "... wherein in the case where an interrupt signal based on one of a plurality of interrupt factors is supplied to the microprocessor, pulse number control data that is set in advance corresponding to the supplied interrupt factor..."

For examination purposes, claim 7 has been interpreted as "...setting pulse number control data that is set in advance corresponding to interrupt factors..."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3-6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim[1] in view of McKenzie et al [McKenzie] US Pat No 5881297.

10. Referring to claim 1, Kim teaches the invention including:

[1] As cited in the previous office action.

a. A clock control device which controls the number of pulses of an operation clock to a microprocessor at least based on whether or not there is a bus busy signal indicating a bus busy state from said microprocessor [abstract and col. 1 lines 10-15].

b. clock control means which supplies the microprocessor with a system clock while the bus busy signal is existing and which supplies the microprocessor with a clock having a reduced number of pulses while said bus busy signal is not existing, respectively as an operation clock [col. 2 lines 55-67].

Although Kim teaches supplying a clock with reduced frequency to a microprocessor while a bus busy signal exists, it is not explicitly taught that the clock has a reduced number of pulses of the system clock. In fact, Kim does not explicitly teach how or in what manner it frequency is reduced. McKenzie teaches reducing an effective frequency of a clock signal in a plurality of different ways including clock dividing and clock gating [238, 240 and 242 fig. 4B]. When reducing an effective frequency by gating a clock, McKenzie teaches using a counter to control when to block an input clock from being output. In particular, when in a reduced frequency mode, the McKenzie system starts a counter, whenever the count value reaches "0", the input clock is allowed to pass through as the output clock. This enables the system to essentially reduce the frequency of the input clock being provided to components within a system by outputting a clock pulse every 2, 3, 4, etc... clock cycles depending on what a count value of the counter is set to [fig. 6 and col. 6 lines 10-22]. It would have been obvious to one of ordinary skill in the art to include the clock gating means taught by McKenzie into the Kim system because it provides one of a plurality of ways to reduce the clock frequency to the processor during a bus busy state.

11. Referring to claim 3, Kim teaches reducing a processor clock to a predetermined value based on whether the system is to enter a lower power mode or if an I/O device is to utilize the bus [col. 1 lines 27-30 and 46-56 and col. 1 line 66-col. 2 line 10]. Indicating a lower power mode or that another I/O device is to utilize the bus is interpreted as being performed by interrupts since interrupts are triggered when a systems current operation is to be interrupted. Because Kim teaches reducing the clock to the processor by a preset value (e.g. ½, ¼ or to a value below a certain threshold), the clock value is interpreted as being set in advance.

12. Referring to claims 4-6 and 8 these are rejected on the same basis as set forth hereinabove. Kim teaches the device and therefore teaches the method performed by the device.

13. Claims 2, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and McKenzie as applied to claims 1, 3-6 and 8 above, and further in view of Tanenbaum[2].

14. Referring to claim 2, although Kim teaches the system and method for controlling a clock supplied to a processor based on an identified interrupt factor, it is not explicitly taught that this can be performed via software. Rather, Kim suggests the above being performed using a bus controller [col. 2 lines 1-10 and 40-48]. In summary, Kim teaches the system for adjusting a clock being supplied to a processor based on one of a plurality of instances which include, entering a doze, standby or suspend mode or when another device requests usage of the bus. Each of the instances adjust the clock in a separate but distinctive manner such as reducing the clock to ½ or ¼ its speed or setting the clock speed below a certain threshold as stated above. Since the Bus controller explicitly controls the clock speed to the processor, it is interpreted that the bus controller identifies and distinguishes between each separate instance (i.e. interpreted as

receiving and distinguishing between different interrupts as stated above) and sends an adjustment signal to the clock generator accordingly. Tanenbaum explicitly teaches "hardware and software are logically equivalent" [page 11]. In particular, Tanenbaum teaches that anything done in hardware can also be performed through software. Therefore, it would have been obvious to modify the Kim system to identify the different instances (i.e. distinguish between the different interrupts) through software because it would reduce the cost and complexity of the bus controller in that it would no longer have to include hardware for identifying the different interrupts. Because the Kim-Tanenbaum system identifies the interrupts through software, and because the processor executes software, it is obvious that the processor would receive the interrupt signals. Then, the software executing on the processor would identify the type of interrupt and send a corresponding clock control signal (i.e. pulse number control data) to the bus controller/clock generator (i.e. clock control means) for controlling the clock supplied to the processor.

15. Referring to claims 7 and 9, these are rejected on the same basis as set forth hereinabove.

Response to Arguments

16. Applicant's arguments filed 5/21/07 have been fully considered but they are not persuasive.

17. Applicants argue in substance that applicants use of the term random gap is appropriate because "it is not necessary that the application describe the claim limitations exactly" and that "a patentee can be his own lexicographer provided the patentee's definition, to the extent it differs from the conventional definition, is clearly set forth in the specification." Furthermore, it

---

[2] As cited in the previous office action.

is argued that the specification as quoted by applicant[3] covering details beginning at page 9, line 21 - page 10, line 10 clearly demonstrates applicants possession of this random gap usage.

18. In response to applicants argument that the specification does not have to describe the claim limitations exactly is refuted by applicants own admission stating that, for a patentee to be their own lexicographer, the extent the patentees definition differs from a conventional definition must clearly set forth the definition in the specification. In summary, applicant can not argue that the specification does not have to describe the random gap associated with the clock signal while at the same time state that applicants definition of the random gap must be clearly set forth in the specification.

In addition, applicants attempt to single out a portion of the specification to refer to what applicant believes to be a random gap, has absolutely nothing in common with the random gap associated when a bus busy signal is existing as claimed. Rather, applicant decides to refer to a portion of the specification which teaches how a system clock is supplied unconditionally to a processor when a bus busy signal is existing (i.e. when the bus is NOT busy). Rather, it is believed that applicant intention was to refer to page 10, lines 11-19 which illustrates how a system clock is generated periodically when the bus is busy and is obtained as the microprocessor clock. Even if the examiners assumptions are true, there is still no clear definition in the specification as to how there is any sort of randomness associated with the periodic generation of the system clock. By definition, random refers to being without definite pattern. Periodic on the other hand has an explicit pattern as is seen in applicants Fig. 2 when a bus busy signal is equal to "0". Clearly, the microprocessor clock is a periodic clock signal, which provides a clock pulse on every other clock pulse of the system clock. Because there is no

[3] See page 9 of the REMARKS filed 5/21/07.

clear definition that a clock having a random gap refers to this periodic clock signal (which is completely contrary to the definition of random) as necessitated under applicants own admission, the applicant has not fulfilled the written description requirement and the rejections/objections associated with applicants usage of a random gap is maintained.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Connolly
Examiner
Art Unit 2115

mc
July 31, 2007